WHAT IS CLAIMED IS:

1. A processor system that includes a dynamic translation facility and that runs a binary-coded program oriented to an incompatible platform while dynamically translating instructions, which constitute the program, into instruction binary codes understandable by itself, comprising:

a processing flow for fetching the instructions, which constitute the binary-coded program oriented to an incompatible platform, one by one, and interpreting the instructions one by one using software; and

a processing flow for translating respective of the instructions into an instruction binary code understandable by itself when necessary, storing the instruction binary code, and optimizing the instruction binary code being stored when necessary,

wherein:

the processing flow for interpreting the instructions and the processing flow for translating are independent and processed in parallel with each other.

2. A processor system according to Claim 1, wherein:

during optimization of respective instruction binary code, new instruction binary codes are arranged to produce a plurality of processing flows so that iteration or procedure call can be executed in parallel with each other.

3. A processor system according to Claim 1, wherein:

a processing flow for prefetching the binary-coded program oriented to the incompatible platform into a cache memory is defined separately from the processing flow for interpreting and the processing flow for translating and optimizing; and

the processing flow for prefetching is processed in parallel with the processing flow for interpreting and the processing flow for translating and optimizing.

4. A processor system according to Claim 1, wherein:

every time translation and optimization of an instruction binary code of a predetermined unit is completed within the processing flow for translating and optimizing, the optimized and translated instruction binary code is exchanged for an instruction code that is processed within the processing flow for interpreting at the time of completion of optimization; and

when the instructions constituting the binary-coded program oriented to the incompatible platform are being interpreted one by one within the processing flow for interpreting, in case that an optimized translated instruction binary code corresponding to one instruction is present, the optimized translated instruction binary code is executed.

5. A processor system according to Claim 1, wherein the

processor system is implemented in a chip multiprocessor that has a plurality of microprocessors mounted on one LSI chip, and the different microprocessors process the plurality of processing flows in parallel with one another.

6. A processor system according to Claim 1, wherein one instruction execution control unit processes a plurality of processing flows concurrently, and the plurality of processing flows are processed in parallel with one another.

7. A processor system according to Claim 1, wherein when a translated instruction being processed within the processing flow for interpreting is exchanged for a new translated instruction produced by optimizing the translated instruction within the processing flow for translating and optimizing, an exclusive control is performed.

8. A processor system including a dynamic translation facility and including at least one processing flow, wherein:

the at least one processing flow includes a first processing flow for sequentially prefetching a plurality of instructions, which constitute a binary-coded program to be run in incompatible hardware, and storing the instructions in a common memory, a second processing flow for concurrently interpreting the plurality of instructions stored in the common memory in parallel

with one another, and a third processing flow for translating the plurality of interpreted instructions.

9. A processor system according to Claim 8, wherein the second processing flow executes the translated code when the instruction of the plurality of instructions have already been translated and interprets the instruction when it has not been translated.

10. A processor system according to Claim 8, wherein within the third processing flow, among the plurality of instructions, instructions that have not been translated are translated, and the translated instructions are re-sorted or the number of translated instructions is decreased.

11. A processor system according to Claim 8, wherein the first processing flow, the second processing flow, and the third processing flow are processed independently in parallel with one another.

12. A semiconductor device having at least one microprocessor, a bus, and a common memory, including:

the at least one microprocessor composed of processing at least one processing flow;

the at least one processing flow including:

a first processing flow for sequentially prefetching a plurality of instructions that constitute a binary-coded program to be run in incompatible hardware, and storing the instructions in the common memory,

a second processing flow for concurrently interpreting the plurality of instructions stored in the common memory in parallel with one another, and

a third processing flow for translating the plurality of interpreted instructions,

wherein:

the at least one microprocessor is composed of implementing the plurality of instructions in parallel with one another.

13. A binary translation program for making a computer perform in parallel:

a step for performing fetching of a plurality of instructions into the computer;

a step for translating instructions, which have not been translated, among the plurality of instructions; and

a step for executing the instructions through the step for translating.